Amendment Of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing Of Claims:

1. (Currently Amended) A level shifting circuit comprising:

a first MOS transistor having a gate whose first terminal is connected to a first port and whose second terminal is connected to a second port,

a second MOS transistor of the same conductivity type as the first MOS transistor, whose first terminal is connected to a power supply voltage terminal that supplies a power supply voltage corresponding to a reference logic level and whose second terminal and gate terminal are both connected to the gate terminal of the first MOS transistor[.], and wherein a voltage transition at the first port from substantially a reference voltage to a first voltage is coupled to the gate of the first transistor by gate to first terminal capacitance to switch a mode of operation of the level shifting circuit to clamp the gate voltage of the first transistor;

a bias means for supplying a prescribed bias voltage below the power supply voltage to the gate terminal of the first MOS transistor.

2. (previously presented) The level shifting circuit of Claim 1, comprising a first clamping circuit connected between the power supply voltage terminal and the first port in order to clamp the potential at the first port close to the reference logic level.

3. (currently amended) A level shifting circuit comprising

a first MOS transistor whose first terminal is connected to a first port and whose second terminal is connected to a second port,

a second MOS transistor of the same conductivity type as the first MOS transistor, whose first terminal is connected to a power supply voltage terminal that supplies a power supply voltage corresponding to a reference logic level and whose second terminal and gate terminal are both connected to the gate terminal of the first MOS transistor,

a bias means for supplying a prescribed bias voltage below the power supply voltage to the gate terminal of the first MOS transistor,

wherein the first clamping circuit comprises [the level shifting circuit of Claim 1, comprising] a first switch which [wherein the first clamping circuit] is turned off when the potential levels of the first and second ports have logic levels different from the reference logic level, and it is turned on when the potential of one of the first and the second port has a logic level equal to the reference logic level.

4. (currently amended) The level shifting circuit of Claim [2] 3, wherein the first clamping circuit is provided with a first diode for allowing a current to flow in the forward direction from the power supply voltage terminal to the first port.

5. (currently amended) The level shifting circuit of Claim [2] 4, wherein the first clamping circuit is provided with a first constant current source circuit for allowing a constant current to flow from the power supply voltage terminal to the first port.

6. (currently amended) The level shifting circuit of Claim [1] 5 comprising a second clamping circuit connected between the power supply voltage terminal and the second port in order to clamp the potential of the second port near the reference logic level.

7. (Currently Amended) The level shifting circuit of Claim 6, [further comprising] wherein the second clamping circuit comprises a second switch which [wherein the second clamping circuit] is turned off when the potential levels of the first and the second ports have logic levels different from the reference logic level, and it is turned on when the potential of one of the and the second ports is logically equal to the [aforementioned] reference logic level.

8. (currently Amended) The level shifting circuit of Claim [6] 7, wherein the second clamping circuit is provided with a second diode for allowing a current to flow in the forward direction from the power supply voltage terminal to the second port.

9. (previously presented) The level shifting circuit of described under Claim 6, wherein the second clamping circuit is provided with a second constant current source circuit for allowing a constant current to flow from the power supply voltage terminal to the second port.

10. (currently amended) The level shifting circuit of Claim [1] 8, further comprising a third diode whose anode is connected to the first port, and whose cathode is connected to the gate terminal of the first MOS transistor.

11. (previously presented) The level shifting circuit of Claim 10, furthercomprising a first resistor connected in series with the third diode between the first port and the gate terminal of the first MOS transistor.

12. (currently amended) The level shifting circuit of Claim [10], 11, furthercomprising a third constant current source circuit connected in series with the third diode between the first port and the gate terminal of the first MOS transistor.

13. (currently amended) The level shifting circuit of Claim [1] 11, further comprising a fourth diode whose anode is connected to the second port, and whose cathode is connected to the gate terminal of the first MOS transistor.

14. (previously presented) The level shifting circuit of Claim 13, further comprising a second resistor connected in series with the fourth diode between the second port and the gate terminal of the first MOS transistor.

15. (cancelled)

16. (currently amended) The level shifting circuit of Claim [1] 13, wherein the bias means is provided with a fifth diode whose anode is connected to the power supply voltage terminal, and whose cathode is connected to the gate terminal of the first MOS transistor.

17. (previously presented) The level shifting circuit of Claim 16, further comprising a third switch connected in series with the fifth diode the power supply voltage terminal and the gate terminal of the first MOS transistor,

a fourth switch connected between the gate terminal of the first MOS transistor and a reference potential logic level different from the reference logic level, and

a switch control means that turns the third switch on and the fourth switch off and vice versa.

18. (previously presented) The level shifting circuit of Claim 17 further comprising a voltage amplifier which increases the potential of the gate terminal of the first MOS transistor to a level higher than the power supply voltage in response to a control signal given by the switch control means in order to turn the third switch on and turn the fourth switch off.

19. (previously presented) The level shifting circuit of Claim 18, wherein the voltage amplifier circuit is provided with a delayed voltage output circuit that increases its output voltage from a logic level different from the reference logic level to a logic level equal to the reference logic level after a prescribed delay time has passed after the control signal is input, as well as with a capacitor connected between the output terminal of the delayed voltage output circuit and the gate terminal of the first MOS transistor.

20. (currently amended) The level shifting circuit of Claim [1] 17, further comprising a third MOS transistor whose first terminal is connected to the first port and whose second terminal is connected to the second port,

a fourth MOS transistor of the same conductivity type as the third MOS transistor whose first terminal is connected to the power supply voltage terminal and whose second terminal and gate terminal are both connected to the gate terminal of the third MOS transistor,

a sixth diode whose anode is [connected] coupled to the power supply voltage terminal and whose cathode is connected to the gate terminal of the third MOS transistor,

a fifth switch connected in series with the sixth diode between the power supply voltage terminal and the gate terminal of the third MOS transistor,

a sixth switch connected between the gate terminal of the third MOS transistor and a reference potential having a logic level different from the reference logic level,

a switch control means that turns the fifth switch on and the sixth switch off and vice versa, and

a voltage amplifier that increases the potential of the gate terminal of the third MOS transistor to a level higher than the power supply voltage in response to a control signal given by the switch control means in order to turn the fifth switch on and turn the sixth switch off.

21. (previously presented) The level shifting circuit of Claim 20, wherein the voltage amplifier is provided with a delayed voltage output circuit that increases its output voltage from a logic level different from the reference logic level to a logic level equal to the reference logic level after a prescribed amount of delay time has passed after the control signal is input, as well as with a capacitor connected between the output terminal of the delayed voltage output circuit and the gate terminal of the third MOS transistor.

22. (previously presented) A level shifting circuit comprising a first MOS transistor connected between a first input/output terminal and a second input/output terminal,

a second MOS transistor connected between a first power supply voltage terminal and the gate terminal of the first MOS transistor and whose gate terminal is connected to the gate terminal of the first MOS transistor,

a first rectifying element connected between a first power supply voltage terminal and the gate terminal of the first MOS transistor in order to source current from the first power supply voltage terminal to the gate terminal of the first MOS transistor,

a second rectifying element connected between the first input/output terminal and the gate terminal of the first MOS transistor in order to source current from the first input/output terminal to the gate terminal of the first MOS transistor,

a third rectifying element connected between the second input/output terminal and the gate terminal of the first MOS transistor in order to source current from the second input/output terminal to the gate terminal of the first MOS transistor,

a third MOS transistor connected between the first power supply voltage terminal and the first input/output terminal,

a fourth rectifying element connected between the third MOS transistor and the first input/output terminal in order to source current from the first power supply voltage terminal to the first input/output terminal,

a fourth MOS transistor connected between the first power supply voltage terminal and the second input/output terminal,

a fifth rectifying element connected between the fourth MOS transistor and the second input/output terminal in order to source current from the first power supply voltage terminal to the second input/output terminal, and

a logic circuit whose first and second input terminals are connected to the first and the second input/output terminals, respectively, in order to output a control signal to turn on the fourth and fifth MOS transistors when the voltage level of the first and/or the second input/output terminal corresponds to the power supply voltage.

23. (previously presented) The level shifting circuit of Claim 22, wherein the first and second MOS transistors are NMOS transistors,

the third and fourth MOS transistors are PMOS transistors,

the first rectifying element is a diode whose anode is connected to the first power supply voltage terminal and whose cathode is connected to the gate terminal of the first MOS transistor,

the second rectifying element is a diode whose anode is connected to the first input/output terminal and whose cathode is connected to the gate terminal of the first MOS transistor,

the third rectifying element is a diode whose anode is connected to the second input/output terminal and whose cathode is connected to the gate terminal of the first MOS transistor,

the fourth rectifying element is a diode whose anode is connected to the third MOS transistor and whose cathode is connected to the first input/output terminal, and

the fifth rectifying element is a diode whose anode is connected to the fourth MOS transistor and whose cathode is connected to the second input/output terminal.

24. (previously presented) The level shifting circuit of Claim 22, comprising

a fifth MOS transistor connected between the first rectifying element and the gate terminal of the first MOS transistor in order to cut off the current path formed between the first rectifying element and the gate terminal of the first MOS transistor, the current path between the second rectifying element and the gate terminal of the first MOS transistor, and the current path between the third rectifying element and the gate terminal of the first MOS transistor,

a sixth MOS transistor connected between the gate terminal of the first MOS transistor and the second power supply voltage terminal, and

a control circuit that supplies a control signal in order to make the fifth MOS transistor and the sixth MOS transistor conductive in a complementary manner.

25. (New) The level shifting circuit of Claim 1 comprising a second clamping circuit connected between the power supply voltage terminal and the second port in order to clamp the potential of the second port near the reference logic level.